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10/002,461	11/01/2001	Keith R. Slavin	DB000955-000	5286

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EXAMINER	
ELMORE, REBA I	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 10/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,461	SLAVIN, KEITH R.	
	Examiner	Art Unit	
	Reba I. Elmore	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38 and 41-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38 and 41-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-38 and 41-44 are presented for examination.

2. Prosecution on the merits of this application is reopened on claims 1-44 considered unpatentable for the reasons indicated below in the rejection of claim 1-44 as being anticipated by Allan et al. as detailed.

SPECIFICATION

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 1-38 and 41-44 are rejected under 35 U.S.C. 102(e) as being anticipated by Allen et al.

6. Allan teaches the invention (claim 1) as claimed including a method comprising:

inputting an input word to a plurality of hash circuits, each hash circuit being responsive to a different portion of the input word as comparing a desired search term against a list of

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entries simultaneously by using an Internet router having a CAM for searching specified address data (e.g., see col. 1, line 31 to col. 2, line 7 and Figure 6 and col. 7, line 50 to col. 8, line 50);

outputting a hash signal from each hash circuit (e.g., see Figure 6);

enabling portions of a CAM in response to the hash signals (e.g., see col. 8, lines 13-50);

inputting the input word to the CAM (e.g., see Figure 6);

comparing the input word in the enabled portions of the CAM (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50); and,

outputting information responsive to the comparing (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

As to claim 2, Allan teaches assigning a mask to each hash circuit such that each hash circuit is responsive to a different n-bit portion of the input word with the mask being equivalent to the configuration register used to perform the block select for the search function (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

As to claim 3, Allan teaches inputting the least significant n bits of the input word to a memory, and wherein the outputting includes selecting between information responsive to a match being found in the memory and information responsive to a match being found in the CAM (e.g., see col. 7, lines 50-62).

As to claim 4, Allan teaches delaying the inputting the input word to the CAM until the enabling is completed as being inherent as the section of the CAM being searched must be precharged prior to the actual access of the required part of the CAM (e.g., see col. 2, line 45 to col. 3, line 38).

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As to claim 5, Allan teaches the enabling includes using the hash signals to select from a plurality of stored signals and using the selected stored signals to enable a portion of the CAM (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

As to claim 6, Allan teaches the selected stored signals includes using a starting index and a run length with the index being the bytes in the configuration register and the selection of the number of memory block to be searched (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

As to claim 7, Allan teaches using the selected stored signals includes using a starting index and an ending index with the index being the bytes in the configuration register and the ending index being equivalent to the number of memory block to be searched (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

7. Allan teaches the invention (claim 8) as claimed including a method of operation a CAM comprising:

hashing a comparand word as comparing a desired search term against a list of entries simultaneously by using an Internet router having a CAM for searching specified address data (e.g., see col. 1, line 31 to col. 2, line 7);

precharging certain portions of a CAM in response to the hashing as enabling portions of a CAM dependent upon the hashing function (e.g., see col. 8, lines 13-50); and,

inputting the comparand word to the CAM as providing the search data to the search port (e.g., see Figure 6 and col. 8, lines 28-50).

As to claim 9, Allan teaches the hashing includes hashing different n–bit portions of the comparand word (e.g., see col. 7, lines 21-49).

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As to claim 10, Allan teaches inputting the least significant n bits of the comparand word to a memory and outputting information responsive to a match being found either in the memory or the CAM as an embodiment which places entries within predictable locations with the CAM (e.g., see col. 7, lines 50-62).

As to claim 11, Allan teaches delaying the inputting of the comparand word to the CAM until the precharging is completed as being inherent as the section of the CAM being searched must be precharged prior to the actual access of the required part of the CAM (e.g., see col. 2, line 45 to col. 3, line 38).

As to claim 12, Allan teaches the precharging includes using the hash signals to select from a plurality of stored signals and using the selected stored signals to precharge portions of the CAM (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

As to claim 13, Allan teaches using the selected stored signals includes using a starting index and a run length with the index being the bytes in the configuration register and the selection of the number of memory block to be searched (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

As to claim 14, Allan teaches using the selected stored signals includes using a starting index and an ending index with the index being the bytes in the configuration register and the ending index being equivalent to the number of memory block to be searched (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

8. Allan teaches the invention (claim 15) as claimed including a method of operating a CAM for processing address information comprising:

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inputting an Internet address to a plurality of hash circuits, each hash circuit being responsive to a different portion of the address as comparing a desired search term against a list of entries simultaneously by using an Internet router having a CAM for searching specified address data (e.g., see col. 1, line 31 to col. 2, line 7 and Figure 6 and col. 7, line 50 to col. 8, line 50);

outputting a hash signal from each hash circuit (e.g., see col. 8, lines 13-50);

using the hash signal to identify portion of a CAM (e.g., see Figures 5A-5B);

inputting the address to the CAM (e.g., see Figures 5A-5B);

comparing the address in only the identified portions of the CAM as hashing a comparand word as comparing a desired search term against a list of entries in the CAM for searching specified address data (e.g., see col. 1, lines 31 to col. 2, line 7); and,

outputting port information in response to a match being found in the CAM (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

As to claim 16, Allan teaches assigning a mask to each hash circuit such that each hash circuit is responsive to a different n-bit portion of the address with the mask being equivalent to the configuration register used to perform the block select for the search function (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

As to claim 17, Allan teaches inputting the least significant n bits of the address to a memory wherein the outputting includes selecting between port information associated with a match in the memory and port information associated with a match in the CAM (e.g., see col. 7, lines 50-62).

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As to claim 18, Allan teaches delaying the inputting of the address to the CAM until portions of the CAM have been precharged in response to the hash signals as being inherent as the section of the CAM being searched must be precharged prior to the actual access of the required part of the CAM (e.g., see col. 2, line 45 to col. 3, line 38).

As to claim 19, Allan teaches using the hash signals includes selecting from a plurality of stored signals and using the selected stored signals to precharge portions of the CAM (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

As to claim 20, Allan teaches using the selected stored signals includes using a starting index and a run length with the index being the bytes in the configuration register and the selection of the number of memory block to be searched (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

As to claim 21, Allan teaches using the selected stored signals includes using a starting index and an ending index with the index being the bytes in the configuration register and the ending index being equivalent to the number of memory block to be searched (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

9. Allan teaches the invention (claim 22) as claimed including a method of operation a CAM for processing address information comprising:

hashing different prefixes with an Internet address as using different part of the configuration register (e.g., see Figure 5A-5B);

precharging certain portions of a CAM in response to the hashing (e.g., see col. 8, lines 13-50);

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comparing the Internet address in the precharged portions of the CAM (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50); and,

outputting information in response to a match being found in the CAM (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

As to claim 23, Allan teaches inputting the least significant n bits of the address to a memory wherein the outputting information includes selecting between information associated with a match in the memory and information associated with a match in the CAM as an embodiment which places entries within predictable locations with the CAM (e.g., see col. 7, lines 50-62).

As to claim 24, Allan teaches delaying the comparing until the precharging is completed as being inherent as the section of the CAM being searched must be precharged prior to the actual access of the required part of the CAM (e.g., see col. 2, line 45 to col. 3, line 38).

As to claim 25, Allan teaches the precharging includes using the hash signals to select from a plurality of stored signals and using the selected stored signals to precharge portions of the CAM (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

As to claim 26, Allan teaches using the selected stored signals includes using a starting index and a run length with the index being the bytes in the configuration register and the selection of the number of memory block to be searched (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

As to claim 27, Allan teaches using the selected stored signals includes using a starting index and an ending index with the index being the bytes in the configuration register and the

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ending index being equivalent to the number of memory block to be searched (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

10. Allan teaches the invention (claim 28) as claimed including a circuit comprising:

a CAM for receiving a comparand word (e.g., see Figure 3);

a plurality of hash circuits connected in parallel, each for producing a hash signal in response to a portion of the comparand word (e.g., see Figure 6); and,

a circuit, responsive to the hash signals, for precharging portions of the CAM (e.g., see col. 8, lines 28-50);

As to claim 29, Allan teaches the circuit responsive to the hash signals includes a plurality of memory devices responsive to the hash signals and enable logic responsive to the plurality of memories (e.g., see Figures 3-6).

As to claim 30, Allan teaches the plurality of memory devices includes a plurality of SRAMs as being inherent as the reference does not address in any way or method refresh circuitry for the CAM thereby requiring nonvolatile memory, i.e. static RAM.

As to claim 31, Allan teaches an output memory device responsive to the CAM for outputting information in responsive to a match in the CAM as an embodiment which places entries in predictable locations within the CAM (e.g., see col. 7, lines 50-62).

As to claim 32, Allan teaches an input memory devices responsive to a portion of the comparand word and a switch response to the input memory devices and the output memory device as using the configuration register with the capability of using a portion of the configuration register for the input (e.g., see Figures 3-7C).

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As to claim 33, Allan teaches a processor, the CAM, the plurality of hash circuits and the circuit responsive to the hash circuit receiving information from the processor (e.g., see Figures 3-7C).

11. Allan teaches the invention (claim 34) as claimed including a circuit comprising:

a CAM (e.g., see (e.g., see Figures 3-7C).

a plurality of hash circuits each for producing a hash signal in response to a portion of a comparand word (e.g., see Figures 3-7C).

a plurality of memory devices responsive to the hash circuits (e.g., see Figures 3-7C).

an enable logic, responsive to the plurality of memory devices, for enabling portions of the CAM as enabling portions of a CAM dependent upon the hashing function (e.g., see col. 8, lines 13-50); and,

a delay circuit for inputting the comparand word to the CAM as being inherent as the section of the CAM being searched must be precharged prior to the actual access of the required part of the CAM (e.g., see col. 2, line 45 to col. 3, line 38).

As to claim 35, Allan teaches the plurality of memory devices includes a plurality of SRAMs as being inherent as the reference does not address in any way or method refresh circuitry for the CAM thereby requiring nonvolatile memory, i.e. static RAM.

As to claim 36, Allan teaches an output memory devices responsive to the CAM for outputting information in response to a match in the CAM as an embodiment which places entries within predictable locations with the CAM (e.g., see col. 7, lines 50-62).

As to claim 37, Allan teaches an input memory device responsive to a portion of the comparand word and a switch responsive to the input memory device and the output memory

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device as using the configuration register with the capability of using a portion of the configuration register for the input (e.g., see Figures 3-7C).

As to claim 38, Allan teaches a processor for initializing the hash circuits, the plurality of memory devices and the CAM (e.g., see col. 2, line 45 to col. 4, line 3).

12. Allan teaches the invention (claim 41) as claimed including a method of initializing hardware (e.g., see col. 2, line 45 to col. 4, line 3), comprising

transferring network addresses to a CAM based on an index to a hash table (e.g., see Figures 3-7C and col. 1, lines 31-55);

transferring port numbers to an output memory device responsive to the CAM as the CAM being used in an internet router (e.g., see Figures 3-7C and col. 1, lines 31-55);

modifying bit prefix values to obtain a ternary representation as using a ternary CAM (e.g., see col. 1, line 56 to col. 2, line 37);

calculating bank run length information as being equivalent to the sizing of the memory bank details of the CAM array (e.g., see col. 2, line 45 to col. 4, line 3); and,

loading starting address and bank run length information into a plurality of memory devices with the starting address being the bytes in the configuration register and the selection of the number of memory block to be searched (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

As to claim 42, Allan teaches periodically transferring invalid network addresses to the CAM (e.g., see col. 1, line 21 to col. 2, line 42).

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As to claim 43, Allan teaches transferring port information to an SRAM for prefixes below a certain length as the CAM including prefixes in block prior to the targeted block (e.g., see col. 2, line 45 to col. 4, line 3).

As to claim 44, Allan teaches the bank run length information includes one of an end address and an address span and with bytes in the configuration register and the selection of the number of memory blocks to be searched (e.g., see Figure 6 and col. 7, line 50 to col. 8, line 50).

CONCLUSION

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Several prior art references have been cited as being significant to the claimed invention limitations.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on M-TH from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2187, Donald Sparks, can be reached for general questions concerning this application at (571) 272-4201. Additionally, the official fax phone number for the art unit is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2187

October 16, 2005

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